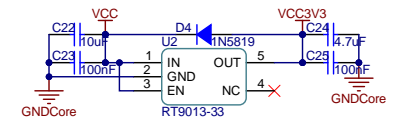
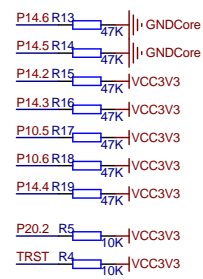


VAREF1:3.3V
VAGND1:GND
VDDM:3.3V
VDD/VDDSB:1.3V
VDD:1.3V
VEXT:3.3V
VDDP3:3.3V
VDDFL3:3.3V
VFLEX:3.3V
VSS:GND
VSSM:GND

默认
HWCFG0=0
HWCFG1=0
HWCFG2=1
HWCFG3=1
HWCFG4=1
HWCFG5=1
HWCFG6=1

| HWCFG[0] P14.6 | HWCFG[1] P14.5 | HWCFG[2] P14.2 | HWCFG[3] P14.3 | HWCFG[4] P10.5 | HWCFG[5] P10.6 | HWCFG[6] P14.4 |
|----------------------------------|--|--|---|--|-------------------|---|
| 0 - SMPS 1 - LDO (default) | 0 - EVR33OFF 1 - EVR33ON (default) | 0 - EVR13OFF 1 - EVR13ON (default) | 0 - Boot from pins 1 - Flash BMI boot (default) | HWCFG[4:5] [0] - Generic Bootstrap (P14.0/1) [1] - ABM, Generic Bootstrap on fail (P14.0/1) [1] - ABM, ASC Bootstrap on fail (P15.2/3) [1] - Internal start from Flash (default) | | Default Pad state 0 - Pins in tristate 1 - Pins with pull-up (default) |

- 1) HWCFG[6] has weak internal pull-up active at start-up if the pin is left unconnected.
- 2) If HWCFG[6] is left unconnected or is externally pulled high, HWCFG[0:5] pins have weak internal pull-ups active at start-up.
- 3) If HWCFG[6] is connected to ground, HWCFG[0:5] pins are in tristate. External pull devices required for all HWCFG pins.
- 4) In packages smaller than QFP144, HWCFG[0:2] pins are absent & internally pulled high ensuring EVR13 (LDO) & EVR33 is active
- 5) HWCFG[0:2] and HWCFG[6] pins are latched during supply ramp-up (VEXT < 2.97V) and stored in PMSWSTAT.HWCFGEVR & TRIST register bits. The remaining HWCFG pins are latched on internal reset release (between 100us - 180us after reset assertion) and stored in STSTAT register.



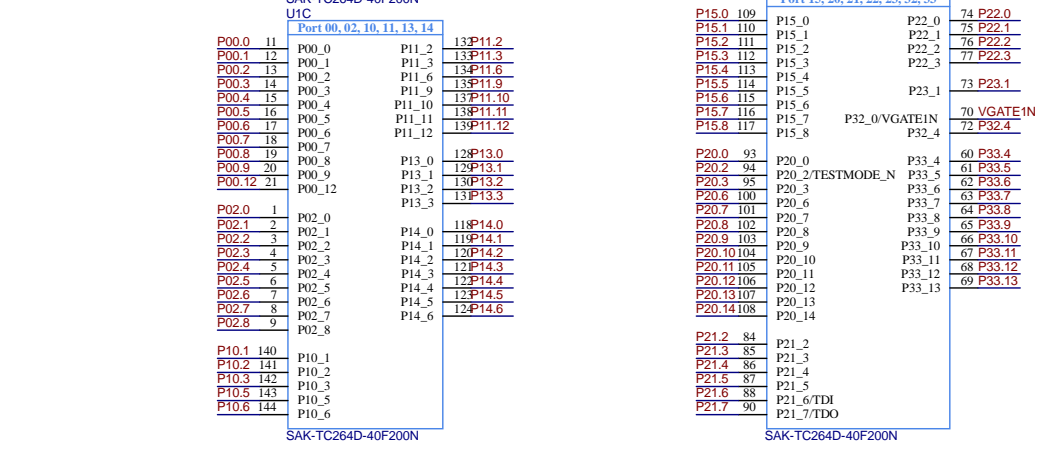
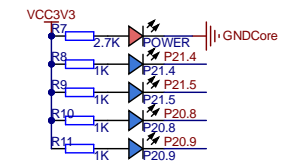
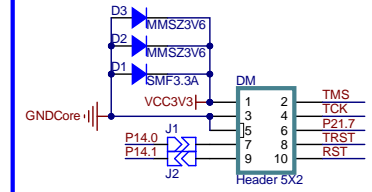
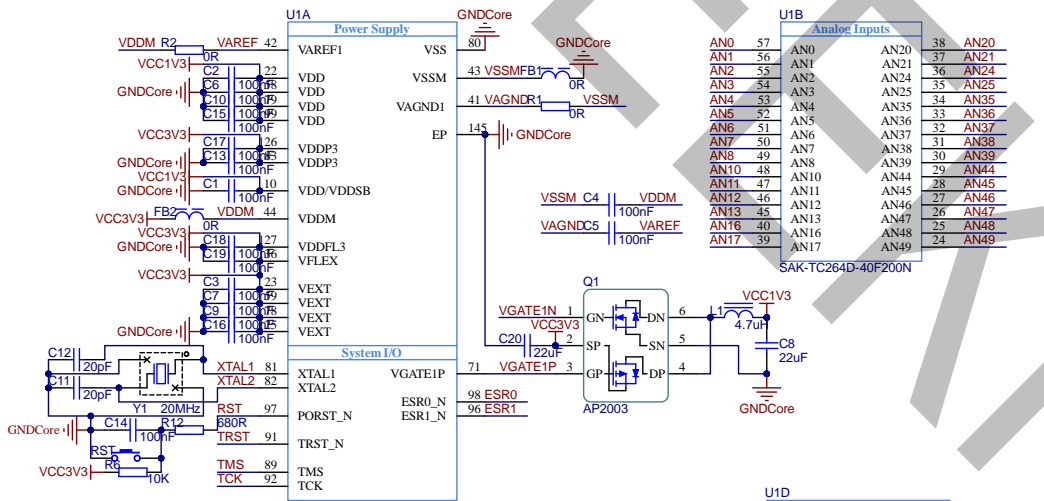
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